AMENDMENTS TO THE CLAIMS

The following is a complete, marked up listing of revised claims with a status identifier in parentheses, underlined text indicating insertions, and strikethrough and/or double-bracketed text indicating deletions.

LISTING OF CLAIMS

1. (CURRENTLY AMENDED) A method of forming a semiconductor device comprising, in order:

implanting a dopant into a substrate to form a source/drain region;

forming a silicide blocking layer on the substrate;

annealing the substrate to activate a portion of the dopant, the annealing being conducted at an anneal temperature T_a;

exposing silicon surfaces on the substrate;

forming silicide layers on the exposed silicon surfaces, the silicide layers being formed at a silicidation temperature T_s, wherein $T_s < T_a$.

2. (ORIGINAL) A method of forming a semiconductor device according to claim 1, wherein:

forming the silicide layers includes depositing a nickel alloy layer on the exposed silicon surfaces, the nickel alloy including nickel and an alloying metal; and

reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer.

3. (ORIGINAL) A method of forming a semiconductor device according to claim 2, wherein:

the lower layer includes at least 95 atomic percent nickel and silicon.

4. (ORIGINAL) A method of forming a semiconductor device according to claim 3, wherein:

the lower layer includes at least 99 atomic percent nickel and silicon.

5. (ORIGINAL) A method of forming a semiconductor device according to claim 4, wherein:

the nickel and silicon are present in the lower layer in an atomic ratio of about 1.

6. (ORIGINAL) A method of forming a semiconductor device according to claim 2, further comprising:

forming a capping layer on the nickel alloy layer before reacting the nickel alloy with the exposed silicon.

7. (ORIGINAL) A method of forming a semiconductor device according to claim 6, wherein:

the capping layer includes a major portion of titanium nitride.

8. (ORIGINAL) A method of forming a semiconductor device according to claim 2, wherein:

the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof, and constitutes no more than about 20 atomic percent of the nickel alloy.

9. (ORIGINAL) A method of forming a semiconductor device according to claim 2, wherein:

the alloying metal is tantalum and is present in a concentration of between about 0.1 and about 10 atomic percent of the nickel alloy.

10. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 9, wherein:

$T_s < 550$ °C[[.]] and $T_a > 750$ °C.

11. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 10, wherein:

T_s is between about 400 and about 530 °C[[.]] and T_a is between about 830 and about 1150 °C.

12. (CURRENTLY AMENDED) A method of forming a semiconductor device comprising, in order:

implanting dopant into a substrate to form a source/drain region;

annealing the substrate to form activated dopant in the source/drain region;

forming a silicide blocking layer on the substrate, thereby deactivating a portion of the activated dopant;

annealing the substrate to reactivate a portion of the deactivated dopant, the annealing being conducted at an anneal temperature T_{pa};

exposing silicon surfaces on the substrate; and

forming silicide layers on the exposed silicon surfaces, the silicide layers being formed at a silicidation temperature T_s, wherein $T_s < T_{pa}$.

13. (ORIGINAL) A method of forming a semiconductor device according to claim 12, wherein:

forming the silicide layers includes depositing a nickel alloy layer on the exposed silicon surfaces, the nickel alloy including nickel and an alloying metal; and

reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer.

14. (ORIGINAL) A method of forming a semiconductor device according to claim 13, wherein:

the lower layer includes at least 95 atomic percent nickel and silicon.

15. (ORIGINAL) A method of forming a semiconductor device according to claim 14, wherein:

the lower layer includes at least 99 atomic percent nickel and silicon.

16. (ORIGINAL) A method of forming a semiconductor device according to claim 15, wherein:

the nickel and silicon are present in the lower layer in an atomic ratio of about1.

17. (ORIGINAL) A method of forming a semiconductor device according to claim 13, further comprising:

forming a capping layer on the nickel alloy layer before reacting the nickel alloy with the exposed silicon.

18. (ORIGINAL) A method of forming a semiconductor device according to claim 17, wherein:

the capping layer includes a major portion of titanium nitride.

19. (ORIGINAL) A method of forming a semiconductor device according to claim 13, wherein:

the alloying metal is at least one metal selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium,

palladium, niobium and combinations thereof, and constitutes no more than about 20 atomic percent of the nickel alloy.

20. (ORIGINAL) A method of forming a semiconductor device according to claim 13, wherein:

the alloying metal is tantalum and is present in a concentration of between about 0.1 and about 10 atomic percent of the nickel alloy.

21. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 20, wherein:

$T_s < 550$ °C[[.]] and $T_{pa} > 750$ °C.

22. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 21, wherein:

T_s is between about 400 and about 530 °C[[.]] and T_{pa} is between about 830 and about 1150 °C.

23. (CURRENTLY AMENDED) A method of forming a semiconductor device comprising, in order:

forming an active region in a semiconductor substrate;

forming a gate electrode structure in the active region;

implanting a first dopant into the active region adjacent the gate electrode structure;

forming spacers adjacent the gate electrode structure;

implanting a second dopant into the active region adjacent the spacers;

forming a silicide blocking layer on the substrate;

annealing the semiconductor substrate at a temperature T_a to activate the first and second dopants;

exposing a silicon surface on the substrate;

forming a metal layer in direct contact with the exposed silicon surface; and

reacting the metal layer with the exposed silicon surface to form~~forming~~ a silicide layer on the silicon surface at a silicidation temperature T_s, wherein $T_s < T_a$.

24. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

forming the silicide layers includes depositing a metal layer on the exposed silicon surfaces, the metal layer being capable of forming a silicide at a silicidation temperature T_s of less than 700 °C.

25. (ORIGINAL) A method of forming a semiconductor device according to claim 23, further comprising:

activating the first and second dopants prior to forming the silicide blocking layer to form activated dopants, wherein the formation of the silicide blocking layer tends to deactivate a portion of the activated dopants.

26. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

the silicide blocking layer is formed at a temperature T_{bl} that is below about 830 °C.

27. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

the silicide blocking layer is formed at a temperature T_{bl} that is between about 535 and about 825 °C.

28. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

the silicide layer is formed at a temperature T_s that is between about 400 and about 530 °C.

29. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

the substrate is annealed at a temperature T_a that is at least about 830 °C.

30. (ORIGINAL) A method of forming a semiconductor device according to claim 23, further comprising:

forming a capping layer on the metal layer before reacting the metal layer with the exposed silicon.

31. (ORIGINAL) A method of forming a semiconductor device according to claim 30, wherein:

the capping layer includes a major portion of titanium nitride.

32. (ORIGINAL) A method of forming a semiconductor device according to claim 23, wherein:

the metal layer is nickel alloyed with one or more minor metals, the minor metals being selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof, wherein the minor metals constitute no more than about 20 atomic percent of the metal layer.

33. (ORIGINAL) A method of forming a semiconductor device according to claim 32, wherein:

the minor metal is tantalum and is present in a concentration of between about 0.1 and about 10 atomic percent of the metal layer.

34. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 32, wherein:

$T_s < 550$ °C[[.]] and $T_a > 750$ °C.

35. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 34, wherein:

T_s is between about 400 and about 530 °C[[.]] and T_a is between about 830 and about 1150 °C.

36. (CURRENTLY AMENDED) A method of forming a semiconductor device according to claim 31, wherein:

the capping layer has a nitrogen:titanium atomic ratio of at least about 0.5.

37. (ORIGINAL) A method of forming a semiconductor device according to claim 33, wherein:

the silicide layer includes a lower layer and an upper layer, the lower layer having a first thickness and the upper layer having a second thickness, and further wherein

the first thickness is at least 70% of a sum of the first thickness and the second thickness.

38. (ORIGINAL) A method of forming a semiconductor device according to claim 37, wherein:

wherein the first thickness is at least 85% of a sum of the first thickness and the second thickness.

39. (ORIGINAL) A method of forming a semiconductor device according to claim 37, wherein:

the lower layer has a tantalum concentration no greater than about 4.9 atomic percent; and

the upper layer has a tantalum concentration of at least about 5 atomic percent.

40. (ORIGINAL) A method of forming a semiconductor device according to claim 39, wherein:

the lower layer has a tantalum concentration no greater than about 0.5 atomic percent; and

the upper layer has a tantalum concentration no greater than about 60 percent.

* * * * *

THE REMAINDER OF THE PAGE HAS BEEN LEFT BLANK INTENTIONALLY